MODEL III

VIDEO DISPLAY GENERATOR LAB

OBJECTIVE:

TO FAMILIARIZE THE FIELD SERVICE REP WITH THE ELECTRICAL OPERATION OF THE MODEL III VIDEO DISPLAY GENERATOR.

UPON COMPLETION OF THIS LAB, THE FIELD SERVICE REP WILL BE ABLE TO:

1) MEASURE AND RECOGNIZE WAVEFORMS ASSOCIATED WITH THE VIDEO DISPLAY GENERATOR CIRCUITRY.

2) RECOGNIZE AND ISOLATE FAULT CONDITIONS ASSOCIATED WITH THE VIDEO DISPLAY GENERATOR.

3) UNDERSTAND THE ELECTRICAL OPERATION OF THE VIDEO DISPLAY GENERATOR.

PREREQUISITE:

MODEL III VIDEO DISPLAY GENERATOR THEORY

EQUIPMENT REQUIRED:

1) DIGITAL VOLTMETER

2) OSCILLOSCOPE

3) LAB TOOL KIT

INTRODUCTION:

IN THIS LAB ASSIGNMENT, YOU WILL BE ASKED TO MEASURE AND RECORD SOME OF THE MOST IMPORTANT WAVEFORMS ASSOCIATED WITH THE VIDEO DISPLAY GENERATOR. YOU WILL ALSO BE REQUIRED TO ANSWER A FEW QUESTIONS CONCERNING THESE MEASUREMENTS.

ALL WAVEFORM MEASUREMENTS WILL BE MADE WITH THE MODEL III IN THE 64 CHARACTER MODE. CERTAIN WAVEFORMS WILL BE MEASURED IN THE 32 CHARACTER MODE. UPON COMPLETING YOUR MEASUREMENTS IN THE 32 CHARACTER MODE, RETURN TO THE 64 CHARACTER MODE BEFORE PROCEEDING TO THE NEXT MEASUREMENT.

DUE TO TIME LIMITATIONS, YOU WILL NOT BE ABLE TO COMPLETE ALL OF THE MEASUREMENTS OUTLINED IN THIS LAB ASSIGNMENT.

DO AS MANY OF THE MEASUREMENTS AS YOU CAN, THEN GO BACK AND ANSWER THE QUESTIONS.

VIDEO DISPLY GENERATOR CIRCUITRY:

THE VIDEO DISPLAY GENERATOR CIRCUITRY OF THE MODEL III CAN BE SUBDIVIDED INTO THE 11 BASIC SECTIONS LISTED BELOW. YOUR ASSIGNMENT IS TO MEASURE AND RECORD THE CONTROLLING SIGNALS OF THESE SUBSECTIONS. THE MEASUREMENTS ARE DESIGNED TO ACQUAINT YOU WITH THE WAVEFORMS ASSOCIATED WITH THESE CIRCUITS.

A BRIEF THEORITICAL OVERVIEW ON EACH OF THE CIRCUITS WILL PRECEED YOUR MEASUREMENTS TO GIVE YOU A BETTER UNDERSTANDING OF THE WAVEFORMS YOU'LL BE MEASURING. USE YOUR SCHEMATICS WHILE PERFORMING THESE MEASUREMENTS.

A) MASTER OSCILLATOR
B) DIVIDER CONDITIONING LOGIC
C) DIVIDER CHAIN
D) MULTIPLEXER LOGIC
E) VIDEO RAM
F) CHARACTER/GRAPHIC GENERATION AND OUTPUT LOGIC
G) WAIT TIMING LOGIC
H) CPU WAIT LOGIC
I) VIDEO BLANKING LOGIC
J) CPU DATA CONTROL LOGIC
K) VERTICAL AND HORIZONTAL SYNC

BASIC OSCILLOSCOPE SETTINGS:

1) CH A: .2V/CM; X10 PROBE
2) CH B: .2V/CM; X10 PROBE
3) CH A - CH B COUPLING: DC
4) ALL OTHER SETTINGS WILL BE SPECIFIED.

MEASUREMENTS:

A) MASTER OSCILLATOR.

THE SIGNALS ASSOCIATED WITH THE MASTER OSCILLATOR ARE

"CLOCK" AND "CLOCK/2". SIGNAL "CLOCK" IS 10.1376 MHZ; ITS CYCLE PERIOD IS 98.6 NSEC. SIGNAL "CLOCK/2" IS 5.0688 MHZ AND ITS CYCLE PERIOD IS 197.2 NSEC.

1) CONNECT THE CH A PROBE TO PIN 3 OF U3 TO MEASURE SIGNAL "CLOCK". CONNECT THE CH B PROBE TO PIN 3 OF U4 TO MEASURE SIGNAL "CLOCK/2".

2) SET THE OSCILLOSCOPE AS FOLLOWS:

   MODE: DUAL
   SWEEP TIME/CM: 0.1 MICROSEC
   TRIGGER MODE: NORM
   TRIGGER SOURCE: INTERNAL, CH A

3) ADJUST THE TRIGGERING LEVEL CONTROL ON THE OSCILLOSCOPE FOR A GOOD PRESENTATION. RECORD YOUR RESULTS BELOW.

QUESTION 1. WHY IS SIGNAL "CLOCK/2" DELAYED WITH RESPECT TO SIGNAL "CLOCK"? ALSO, WHAT IS THE APPROXIMATE DELAY TIME?

ANSWER: _____
_____
_____
_____

B) DIVIDER CONDITIONING LOGIC.

THE DIVIDER CONDITIONING LOGIC CONSISTS OF U4 AND U5. U4 IS A DUAL MULTIPLEXER AND U5 IS A DIVIDE BY 16 COUNTER. U6, WHICH PRODUCES SIGNAL "LATCH", IS ALSO PART OF THIS CIRCUIT.

THE IMPORTANT SIGNALS OF THIS CIRCUIT ARE: "MODSEL", "SHIFT", "C1", "CHAIN" AND "LATCH". SIGNAL "CLRCTR" WILL BE A LOGIC HIGH ONLY DURING POWER-ON RESET.

SIGNAL "SHIFT" IS USED TO GENERATE THE CRT CHARACTER DOTS AND ITS FREQUENCY IS THE SAME AS SIGNAL "CLOCK" IN 64 CHARACTER MODE. SIGNAL "SHIFT" WILL BE THE SAME AS SIGNAL "CLOCK/2" IN 32 CHARACTER MODE.

SIGNAL "C1" WILL BE THE SAME AS SIGNAL "CHAIN" IN 64 CHARACTER MODE. SIGNAL "C1" WILL ALLOW THE VIDEO RAMS TO BE ADDRESED IN A "ONES-INCREMENT". "C1" WILL BE A LOGIC LOW IN 32 CHARACTER MODE AND THE VIDEO RAMS WILL NOW BE ADDRESSED IN A "TWOS-INCREMENT".

SIGNAL "CHAIN" HAS A FREQUENCY OF 633.6 KHZ. IT IS USED AS THE "MASTER CLOCK" FOR THE DIVIER CHAIN.

SIGNAL "MODSEL" SETS THE CHARACTER SIZE ON THE CRT. IT WILL BE A LOGIC LOW IN 64 CHARACTER MODE AND SWITCH TO A LOGIC HIGH WHEN 32 CHARACTER MODE IS SELECTED. THE 32 CHARACTER MODE IS SELECTED WHEN THE <SHIFT> AND <->> KEYS ARE DEPRESSED SIMULTANEOUSLY. THE DISPLAY WILL RETURN TO THE 64 CHARACTER MODE WHEN THE <CLEAR> KEY IS DEPRESSED.

"LATCH" IS USED AS A LOADING AND SYNCHRONIZING SIGNAL. IT IS A NEGATIVE-GOING PULSE, SYNCHRONIZED TO BE ACTIVE BETWEEN CHARACTERS. IN 64 CHARACTER MODE, "LATCH" WILL HAVE A PULSE WIDTH OF 98.6 NSEC AND A PULSE REPETITION TIME OF 788.8 NSEC. IN 32 CHARACTER MODE, THE PERIODS FOR "LATCH" WILL DOUBLE. THE FREQUENCY OF "LATCH" WILL ALWAYS BE ONE-EIGHTH OF THE "SHIFT" FREQUENCY.

1) CONNECT THE CH A PROBE TO PIN 4 OF U4 TO MEASURE SIGNAL "SHIFT". CONNECT THE CH B PROBE TO PIN 6 OF U6 TO MEASURE SIGNAL "LATCH".

2) SET THE OSCILLOSCOPE TO TRIGGER INTERNALLY TO CH B.

3) ADJUST THE TRIGGER LEVEL CONTROL ON THE OSCILLØ- FOR A GOOD PRESENTATION. NOTE THAT THE PERIOD FOR SIGNAL "LATCH" IS EIGTH TIMES THAT OF SIGNAL "SHIFT". RECORD YOUR RESULTS BELOW.

4) SWITCH TO 32 CHARACTER MODE AND REPEAT STEP 3. RECORD YOUR WAVEFORMS BELOW.

QUESTION 1. WHAT IS THE PULSE WIDTH OF SIGNAL "LATCH" IN 32 CHARACTER MODE?

ANSWER: _____

5) SET THE SWEEP TIME/CM CONTROL ON THE OSCILLOSCOPE TO 1 MICROSEC; TRIGGER ON AUTO.

6) CONNECT THE CH A PROBE TO PIN 1 OF U4 TO MEASURE SIGNAL "MODSEL". CONNECT THE CH B PROBE TO PIN 7 OF U4 TO MEASURE SIGNAL "C1". SWITCH BETWEEN 64 AND 32 CHARACTER MODES. CONFIRM THAT SIGNAL "MODSEL" IS A LOGIC LOW IN 64 CHARACTER MODE; AT THE SAME TIME, ALSO CONFIRM THAT SIGNAL "C1" IS 633.6 KHZ. RECORD YOUR RESULTS BELOW.

QUESTION 2. WHILE IN THE 32 CHARACTER MODE, WHAT WAS THE LOGIC LEVEL OF SIGNAL "MODSEL"? DID SIGNAL "C1" CHANGE?

ANSWER: _____

C) DIVIDER CHAIN.

THE DIVIDER CHAIN GENERATES ALL OF THE COLUMN, LINE AND ROW SIGNALS REQUIRED BY THE VIDEO DISPLAY GENERATOR. THE DIVIDER CHAIN CONSISTS OF U56, U20 AND PART OF U1. AND GATES OF U21 ARE ALSO PART OF THIS CIRCUIT. THE AND GATES ARE USED TO SET THE MODULO LEVEL OF EACH OF THE COUNTERS IN THE DIVIDER CHAIN.

THE COLUMN COUNTER HAS A MODULO OF 80. THE LINE AND ROW COUNTERS HAVE MODULO COUNTS OF 12 AND 22, RESPECTIVELY.

THE COLUMN AND ROW SIGNALS ARE USED TO RIPPLE ADDRESS THE VIDEO RAMS DURING THE VIDEO DISPLAY TIME. LINE SIGNALS ARE USED AS THE LSB ADDRESSES FOR THE CHARACTER GENERATOR. THE GRAPHICS MULTIPLEXER ALSO USES THE LINE SIGNALS AS ADDRESSES TO FORM PART OF THE GRAPHICS MATRIX.

THE DIVIDER CHAIN ALSO GENERATES SIGNALS "HDRV" AND "VDRV". THESE SIGNALS ARE USED TO SET THE HORIZONTAL AND VERTICAL BLANKING INTERVALS OF THE DISPLAY. SIGNAL "HDRV" IS BLANKED FOR A PERIOD OF 16 COLUMNS, WHICH LEAVES 64 COLUMNS FOR THE DISPLAY. LIKEWISE, SIGNAL

"VDRV" IS BLANKED FOR A PERIOD OF 6 ROWS, LEAVING A REMAINDER OF 16 ROWS FOR THE DISPLAY. SIGNALS "HDRV" AND "VDRV" WILL ALSO BE USED TO HELP IN CREATING THE HORIZONTAL AND VERTICAL SYNC PULSES.

1) CONNECT THE CH A PROBE TO PIN 8 OF U56 TO MEASURE SIGNAL "HDRV". CONNECT THE CH B PROBE TO PIN 11 OF U21 TO MEASURE SIGNAL "C16".

2) SET THE OSCILLOSCOPE AS FOLLOWS:

   MODE: DUAL
   SWEEP TIME/CM: 5 MICROSEC
   TRIGGER SOURCE: INTERNAL, CH A
   TRIGGER MODE: NORM
   TRIGGER SLOPE: POSITIVE

3) ADJUST THE TRIGGER LEVEL CONTROL ON THE OSCILLOSCOPE FOR A GOOD PRESENTATION. CHECK THAT SIGNAL "HDRV" IS A LOGIC HIGH FOR A PERIOD OF APPROXIMATELY 12.6 MICROSECONDS. RECORD YOUR RESULTS BELOW.

4) POSITION THE SWEEP TIME/CM CONTROL ON THE OSCILLOSCOPE TO 10 MICROSECONDS; ADJUST THE TRIGGER LEVEL FOR A GOOD PRESENTATION. RECORD THE PULSE REPETITION TIME (PRT) OF SIGNAL "HDRV" BELOW. THIS PRT IS THE MODULO 80 RESET FOR THE COLUMN COUNTER.

   NOTE: OBSERVE THE SPIKE ON SIGNAL "C16" WHICH IS JUST ON THE TRAILING EDGE OF SIGNAL "HDRV". THIS IS THE MODULO 80 RESET OF SIGNAL "C16".

CHECK THE MODULO PERIOD OF THE LINE COUNTER.

1) CONNECT THE CH A PROBE TO PIN 5 OF U20 TO MEASURE SIGNAL "L4". CONNECT THE CH B PROBE TO PIN 2 OF U21 TO MEASURE SIGNAL "L8". CONNECT THE EXTERNAL PROBE TO PIN 8 OF U56 TO TRIGGER ON SIGNAL "HDRV".

2) SET THE OSCILLOSCOPE AS FOLLOWS:

SWEEP TIME/CM: 0.2 MILLISECONDS
TRIGGER COUPLING: DC
TRIGGER SOURCE: EXTERNAL
TRIGGER MODE: NORM
TRIGGER SLOPE: NEGATIVE

3) ADJUST THE TRIGGER LEVEL CONTROL ON THE OSCILLOSCOPE FOR A GOOD PRESENTATION. ROTATE THE HORIZONTAL POSITION CONTROL ON THE OSCILLOSCOPE SUCH THAT THE TRAILING EDGE OF SIGNAL "L8" IS ON THE LEFT EDGE OF THE OSCILLOSCOPE GRATICULE.

FOR A MODULO OF 12, THE PERIOD OF SIGNAL "L8" SHOULD BE APPROXIMATELY 757 MICROSECONDS. NOTE THAT SIGNAL "L4" IS BEING RESET ON THE TRAILING EDGE OF SIGNAL "L8". RECORD YOUR RESULTS BELOW.

CHECK THE MODULO PERIOD OF THE ROW COUNTER.

1) CONNECT THE CH A-PROBE TO PIN 8 OF U20 TO MEASURE SIGNAL "VDRV". CONNECT THE CH B PROBE TO PIN 4 OF U21 TO MEASURE SIGNAL "R2".

2) SET THE OSCILLOSCOPE AS FOLLOWS:

SWEEP TIME/CM: 2 MILLISECONDS
TRIGGER COUPLING: DC
TRIGGER SOURCE: INTERNAL, CH A
TRIGGER MODE: NORM
TRIGGER SLOPE: NEGATIVE

3) ADJUST THE TRIGGER LEVEL CONTROL ON THE OSCILLOSCOPE FOR A GOOD PRESENTATION. POSITION THE HORIZONTAL CONTROL SUCH THAT THE DISPLAY BEGINS AT THE LEFT EDGE OF THE OSCILLOSCOPE GRATICULE.

4) FOR A MODULO OF 22, CONFIRM THAT THE PRT OF SIGNAL "VDRV" IS 16.6 MILLISECONDS. ALSO NOTICE THAT THE MODULO 22 RESET IS OCCURRING ON THE TRAILING EDGE OF SIGNAL "VDRV". OBSERVE THAT SIGNAL "R2" IS BEING RESET AT THIS SAME TIME.

5) CONNECT THE CH A PROBE TO PIN 3 OF U21 TO MEASURE SIGNAL "R4". NOTE THAT SIGNAL "R4" IS ALSO BEING RESET ON THE TRAILING EDGE OF SIGNAL "VDRV". RECORD YOUR RESULTS BELOW.

QUESTION 1. WHAT IS THE PULSE WIDTH OF SIGNAL "VDRV"? ALSO, HOW MANY ROWS ARE BEING BLANKED DURING THIS PERIOD?

ANSWER: _____

_____

D) MULTIPLEXER LOGIC.
E) VIDEO BLANKING LOGIC.
F) CPU WAIT LOGIC.

THE MULTIPLEXER LOGIC CIRCUIT CONSISTS OF U69,U70 AND U71. THE MULTIPLEXER LOGIC ALLOWS THE VIDEO RAMS TO BE ADDRESSED FROM THE DIVIDER CHAIN OR THE CPU. THE IMPORTANT SIGNAL OF THIS CIRCUIT IS SIGNAL "RSVID*". SIGNAL "RSVID*" WILL-BE ACTIVE AT A LOGIC LOW ONLY AT THE MOMENT WHEN THE CPU IS ADDRESSING THE VIDEIO RAMS.

IN THE DESIGN SCHEME OF THE MODEL III VIDEO DISPLAY GENERATOR CIRCUITRY, THE DIVIDER CHAIN HAS PRIORITY CONTROL OF THE VIDEO RAMS. IN THE CHARACTER OR GRAPHICS DISPLAY MODES THE CPU ACCESS TO THE VIDEO RAMS WILL BE CONDITIONAL. THE CONDITIONS WILL BE LOGICALLY DETERMINED BY THE VIDEO BLANKING AND CPU WAIT CIRCUITS. SIGNALS "PBLANK*" AND "PWAIT*" ARE THE IMPORTANT SIGNALS OF THESE CIRCUITS.

IN THE VIDEO BLANKING CIRCUIT, SIGNAL "PBLANK*" WILL BE ACTIVE AT A LOGIC LOW UNDER THE FOLLOWING DISPLAY CONDITIONS.

CHARACTER DISPLAY MODE:	DURING THE HORIZONTAL AND VERTICAL BLANKING INTERVALS. BETWEEN ROWS, WHEN SIGNAL "L8" IS ACTIVE AT A LOGIC HIGH.
GRAPHICS DISPLAY MODE:	ONLY DURING THE HORIZONTAL AND VERTICAL BLANKING INTERVALS.

AT ALL OTHER TIMES, OR DURING THE DISPLAY TIMES, SIGNAL "PBLANK*" WILL BE MADE INACTIVE AT A LOGIC HIGH.

WHEN THE CPU WANTS TO ACCESS THE VIDEO RAMS, THE CPU WILL GENERATE SIGNAL "VID*". SIGNAL "VID*" IS APPLIED TO THE CPU WAIT CIRCUIT ALONG WITH SIGNAL "PBLANK*".

DURING THE DISPLAY TIME WHEN SIGNAL "PBLANK*" IS INACTIVE, AN ACTIVE "VID*" SIGNAL WILL CAUSE THE CPU WAIT CIRCUIT TO GENERATE SIGNAL "PWAIT*". SIGNAL "PWAIT*" WILL BE SENT BACK TO THE CPU TO PLACE THE CPU IN A WAIT STATE.

AT THE MOMENT WHEN SIGNAL "PBLANK*" BECOMES ACTIVE, THE CPU WAIT CIRCUIT WILL DISABLE SIGNAL "PWAIT*" AND GENERATE SIGNAL "RSVID*" WHICH IS ROUTED TO THE MULTIPLEXER CIRCUIT. SIGNAL "RSVID*" WILL THEN SWITCH THE MULTIPLEXERS, ALLOWING THE CPU TO ADDRESS THE VIDEO RAMS.

BEGIN YOUR MESUREMENTS AS OUTLINED BELOW.

1) CONNECT THE CH A PROBE TO PIN 6 OF U19 TO MEASURE SIGNAL "PWAIT*". CONNECT THE CH B PROBE TO PIN 6 OF U16 TO MEASURE SIGNAL "RSVID*". CONNECT THE EXTERNAL PROBE TO PIN 12 OF U17 TO TRIGGER ON SIGNAL "PBLANK*".

2) KEY-IN AND RUN THE FOLLOWING SIMPLE LOOP PROGRAM.

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10 PRINT "A"
20 GOTO 10
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3) SET THE OSCILLOSCOPE AS FOLLOWS:

SWEEP TIME/CM: 10 MICROSECONDS
TRIGGER COUPLING: DC
TRIGGER SOURCE: EXTERNAL
TRIGGER MODE: NORM
TRIGGER SLOPE: NEGATIVE

4) ADJUST THE TRIGGER LEVEL ON THE OSCILLLOSCOPE FOR A GOOD PRESENTATION. TRIGGERING MUST BE DONE LOOSELY! CONFIRM THAT SIGNAL "RSVID*" IS ACTIVE ONLY WHEN SIGNAL "PWAIT*" IS INACTIVE AT A LOGIC HIGH. RECORD YOUR RESULTS BELOW.

5) CONNECT THE CH A PROBE TO PIN 10 OF U21 TO MEASURE SIGNAL "HDRV". CONFIRM THAT SIGNAL "RSVID*" IS ACTIVE ONLY WHEN SIGNAL "HDRV" IS ACTIVE. RECALL THAT THE ACTIVE PERIOD OF SIGNAL "HDRV" IS THE HORIZONTAL BLANKING INTERVAL. RECORD YOUR RESULTS BELOW.

QUESTION 1. IN CHARACTER MODE, THE LINES BETWEEN ROWS ARE BLANKED FOR ROW SPACING. DURING THIS TIME, THE CPU IS ALLOWED ACCESS TO THE VIDEO RAMS. EXPLAIN AT WHAT POINTS OF THE VIDEO DISPLAY CIRCUIT WOULD YOU CONNECT YOUR OSCILLOSCOPE TO CONFIRM THIS. INCLUDE YOUR OSCILLOSCOPE SETTINGS.

ANSWER: _____

G) VIDEO RAMS.
H) CPU DATA CONTROL LOGIC.

U81 AND U82 ARE 1K X 4 STATIC RAMS WHICH STORE THE ASCII DATA FOR THE CRT DISPLAY. U67 AND PART OF U19 MAKE UP THE CPU DATA CONTROL LOGIC.

THE IMPORTANT SIGNALS OF THESE CIRCUITS ARE THE VIDEO DATA SIGNALS "VD0" THROUGH "VD7" AND READ-WRITE SIGNALS "VRD*", "VWR*". SIGNALS "VRD*" AND "VWR*" SHOULD BE INACTIVE AT A LOGIC HIGH DURING THE DISPLAY TIME. AT THIS SAME TIME, THE VIDEO RAMS SHOULD BE IN THE READ MODE, OUTPUTTING ASCII DATA TO VIDEO LATCH U68. ALSO U67 SHOULD BE IN THE TRI-STATE CONDITION TO PREVENT THE VIDEO DATA FROM FLOWING BACK ONTO THE SYSTEM DATA BUS.

YOUR WAVEFORM MEASUREMENTS WILL BE MADE DURING THE HORIZONTAL DISPLAY TIME TO CONFIRM THE STATUS OF THESE SIGNALS.

1) DEPRESS THE <BREAK> KEY TO STOP THE PROGRAM THAT IS RUNNING.

2) KEY IN AND RUN THIS NEW PROGRAM:

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10 CLS
20 FOR I = 15360 TO 16383
30 POKE I,65
40 NEXT I
50 GOTO 50
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3) CONNECT THE CH B PROBE TO PIN 8 OF U56 TO MEASURE SIGNAL "HDRV".

4) SET THE OSCILLOSCOPE AS FOLLOWS:

SWEEP TIME/CM: 10 MICROSECONDS
TRIGGER COUPLING: DC
TRIGGER SOURCE: INTERNAL, CH B
TRIGGER SLOPE: NEGATIVE

5) CONNECT THE CH A PROBE TO PINS 3, 18, 4, 17, 7, 14, 8 AND 13 OF VIDEO LATCH U68 TO CHECK THE LOGIC LEVELS OF VIDEO DATA LINES "VD0" THROUGH "VD7". RECORD YOUR RESULTS BELOW.

PIN 3____ PIN 18____ PIN 4____ PIN 17____

PIN 7____ PIN 14____ PIN 8____ PIN 13____

QUESTION 1. WHAT IS THE ASCII CHARACTER OF THIS BINARY CODE?

ANSWER: _____

3) CONNECT THE CH A PROBE TO PINS 9 AND 10 OF U19 TO CONFIRM THAT SIGNALS "VRD*" AND "VWR*" ARE INACTIVE DURING THIS HORIZONTAL DISPLAY TIME. RECORD YOUR COMMENTS BELOW.

4) CONNECT THE CH A PROBE TO PINS 1 AND 19 OF U67. THESE SIGNALS SHOULD BE A LOGIC HIGH TO INDICATE THAT BI-

DIRECTIONAL VIDEO DATA BUFFER IS IN THE TRI-STATE MODE DURING THE HORIZONTAL DISPLAY TIME. RECORD YOUR COMMENTS BELOW.

I) CHARACTER/GRAPHIC GENERATION AND OUTPUT LOGIC.

THE CHARACTER/GRAPHIC GENERATION AND OUTPUT CIRCUIT CONSISTS OF LATCH U68, CHARACTER GENERATOR ROM U36, GRAPHICS MULTIPLEXER AND MATRIX LATCH U54 AND U53.

PARALLEL TO SERIAL SHIFT REGISTER U52 OUTPUTS THE CHARACTER AND GRAPHIC DOT INFORMATION TO THE VIDEO DRIVER CIRCUITS.

SIGNAL "DLYCHAR*" TO THE CHARACTER GENERATOR ROM U36 AND SIGNAL "DLYGRAPHIC*" TO THE GRAPHIC MATRIX BUFFER U53 ORIGINATE AT THE VIDEO DISPLAY STATUS LATCH, U55.

SIGNALS "DLYCHAR*" AND "DLYGRAPHIC*" CAN NOT BE BE ACTIVE SIMULTENUOUSLY. IN THE CHARACTER MODE, SIGNAL "DLYCHAR*" WILL BE ACTIVE AT A LOGIC LOW AND SIGNAL "DLYGRAPHIC*" WILL BE INACTIVE AT A LOGIC HIGH. THE CONVERSE IS TRUE WHILE IN GRAPHICS MODE.

SIGNAL "ENALTSET" IS PROGRAMMED THROUGH SOFTWARE TO ENABLE THE 64 ALTERNATE CHARACTER SET. WHILE IN THIS MODE, PIN 22 OF THE CHARACTER GENERATOR ROM, U36, WILL ALWAYS BE A LOGIC LOW AND PIN 19 WILL ALWAYS BE A LOGIC HIGH.

THE SIGNALS ASSOCIATED WITH THE PARALLEL TO SERIAL SHIFT REGISTER ARE: "DLYBLANK", "LATCH" AND "SHIFT".

SIGNAL "DLYBLANK" PLACES PIN 15 OF U52 AT A LOGIC HIGH DURING THE BLANKING INTERVALS MENTIONED EARLIER. THIS LOGIC STATE WILL INHIBIT DOT LOADS, PLACING PIN 13 AT A LOGIC LOW FOR THE DURATION BECAUSE THE SERIAL INPUT AT PIN 1 IS TIED LOW.

WHEN SIGNAL "LATCH" ARRIVES AT A TIME WHEN SIGNAL "DLYBLANK" IS INACTIVE AT A LOGIC LOW, PIN 15 OF U52 WILL DROP TO A LOGIC LOW FOR THE DURATION OF SIGNAL "LATCH". AT THIS TIME, THE DOT INFORMATION WILL BE LOADED INTO THE PARLLEL TO SERIAL SHIFT REGISTER.

SIGNAL "SHIFT" WILL ALWAYS BE PRESENT AT PIN 7 OF U52, BUT IT WILL BECOME ENABLED WITHIN U52 ONLY WHEN PIN 15 OF U52 BECOMES A LOGIC HIGH. THUS, THE DOT INFORMATION CAN BE SENT OUT SERIALLY ONLY WHEN PIN 15 IS AT A LOGIC HIGH (MEANING, DURING THE DISPLAY TIME). THE RATE AT WHICH THE DOTS ARE SENT OUT WILL DEPEND ON THE CHARACTER DISPLAY MODE SELECTION.

THIS CONCLUDES YOUR OVERVIEW OF THE CHARACTER/GRAPHIC GENERATION AND LOGIC CIRCUITS. PROCEED WITH THE WAVEFORM MEASUREMENTS AS OUTLINED BELOW.

1) CONNECT THE CH A PROBE TO PIN 14 OF U55 TO MEASURE SIGNAL "DLYCHAR*"; THEN CONNECT THE CH A PROBE TO PIN 15 OF U55 TO MEASURE SIGNAL "DLYGRAPHIC*". CONFIRM THAT SIGNALS "DLYCHAR*" AND "DLYGRAPHIC*" ARE NOT AT A LOGIC LOW AT THE SAME TIME. RECORD YOUR RESULTS BELOW.

2) SET THE SWEEP TIME/CM CONTROL ON THE OSCILLOSCOPE TO 0.1 MICROSECOND; INTERNAL TRIGGER TO CH A.

3) CONNECT THE CH A PROBE TO PIN 15 OF U52 TO MEASURE THE LOAD PERIOD. CONNECT THE CH B PROBE TO PIN 13 OF U52 TO MEASURE THE VIDEO OUTPUT.

4) CHECK THAT THE VIDEO OUTPUT IS AT A LOGIC LOW DURING THE LOAD PERIOD. RECORD YOUR RESULTS BELOW.

GRAPHICS MODE MEASUREMENTS.

1) STOP THE PROGRAM BY DEPRESSING THE <BREAK> KEY.

2) LIST THE PROGRAM AND REPLACE LINE 30 WITH THE FOLLOWING LINE:

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30 POKE I, 191
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3) RUN THE PROGRAM AND CONFIRM THAT THE ENTIRE DISPLAY AREA IS ON.

4) CONNECT THE CH A PROBE TO PIN 14 OF U55 TO MEASURE SIGNAL "DLYCHAR*"; THEN CONNECT THE CH B PROBE TO PIN 15 OF U55 TO MEASURE SIGNAL "DLYGRAPHIC*".

5) CHECK THAT SIGNAL "DLYCHAR*" IS INACTIVE AT A LOGIC HIGH WHEN SIGNAL "DLYGRAPHIC*" IS ACTIVE AT A LOGIC LOW. RECORD YOUR RESULTS BELOW.

6) CONNECT THE CH A PROBE TO PINS 6, 10, 5, 11, 4 AND 12 OF GRAPHICS MULTIPLEXER U54. CONFIRM THAT THE LOGIC LEVEL ON EACH OF THE PINS IS AT A LOGIC HIGH. RECORD YOUR RESULTS BELOW.

PIN 6____ PIN 10____ PIN 5____ PIN 11____

PIN 4____ PIN 12____

QUESTION 1. WHAT IS THE HEX VALUE FOR THE BINARY MEASURED IN STEP 6. KEEP IN MIND THAT THE LSB IS ON PIN 6 OF U54.

ANSWER: _____

K) VERTICAL AND HORIZONTAL SYNC CIRCUITS.

THE VERTICAL AND HORIZONTAL SYNC LOGIC CONSISTS OF EXCLUSIVE NOR GATES U22 AND U38. U23 ARE ONE-SHOTS USED TO SET THE PULSE WIDTHS OF THE VERTICAL AND HORIZONTAL SYNC PULSES.

THE EXCLUSIVE NOR GATES ARE PROGRAMMABLE. IN THE VERTICAL SECTION OF THE CIRCUIT, THE GATES ARE PROGRAMMED WITH +5 VOLTS OR GROUND WITH SIGNALS "R1", "R2" AND "R4". THE PROGRAMMED RESULT IS ANDED WITH SIGNAL "VDRV" TO GENERATE THE TRIGGER PULSE FOR ONE-SHOT U23. U23 GENERATES THE VERTICAL SYNC SIGNAL "VSYNC". "VSYNC" IS A NEGATIVE-GOING PULSE WITH A PULSE WIDTH OF 693 MICROSEC. SIGNAL "VSYNC" CAN BE "PULSED POSITIONED" WITH RESPECT TO THE INITIATION OF SIGNAL "VDRV" WITH JUMPERS "D-E-F","K-L-M" AND "G-H-J".

THE HORIZONTAL SECTION OF THE CIRCUIT IS ELECTRICALLY

IDENTICAL TO THE VERTICAL. IN THIS SECTION, HOWEVER, THE ONE-SHOT GENERATES THE HORIZONTAL SYNC PULSE, "HSYNC". "HSYNC IS A POSITIVE-GOING PULSE WITH A PULSE WIDTH OF 8 MICROSEC. LIKE THE VERTICAL SYNC PULSE, THE HORIZONTAL SYNC PULSE CAN BE "PULSED POSITIONED" WITH RESPECT TO THE START OF SIGNAL "HDRV". JUMPERS "V-W-X" AND "BB-CC-DD" SETS THE POSITIONS.

BY "PULSE POSITIONING" THE HORIZONTAL AND VERTICAL SYNC PULSES, THE DISPLAY AREA ON THE CRT CAN BE SHIFTED VERTICALLY OR HORIZONTALLY. THE JUMPERS, THEN, ARE USED TO ELECTRICALLY CENTER THE DISPLAY AREA ON THE CRT.

1) REPOSITION THE HORIZONTAL JUMPERS AND NOTICE HOW THE DISPLAY ON THE CRT SHIFTS HORIZONTALLY.

2) REPEAT STEP 1 WITH THE VERTICAL JUMPERS.

QUESTION 1. WITH RESPECT TO DISPLAY POSITIONING, HOW IS THE DISPLAY EFFECTED WHEN THE CHARACTER DISPLAY MODE IS CHANGED.

ANSWER: _____

_____

_____

3) CONNECT THE CH A PROBE TO PIN 12 OF U39 TO MEASURE SIGNAL "VDRV". CONNECT THE CH B PROBE TO PIN 12 OF U23 TO MEASURE SIGNAL "VSYNC".

4) SET THE OSCILLOSCOPE AS FOLLOWS:

SWEEP TIME/CM: 1 MILLISECOND
TRIGGER SOURCE: INTERNAL, CH A
TRIGGER MODE: NORM
TRIGGER SLOPE: POSITIVE

5) THE LEFT EDGE OF THE OSCILLOSCOPE GRATICULE REPRESENTS THE LEADING EDGE OF SIGNAL "VDRV".

QUESTION 2. WHAT IS THE TIME DIFFERENCE BETWEEN THE LEADING EDGE OF SIGNAL "VDRV" AND THE LEADING EDGE OF SIGNAL "VSYNC"?

ANSWER: _____

QUESTION 3. CONTINUING WITH QUESTION 2. WHAT IS THE TIME DIFFERENCE BETWEEN THE TWO SIGNALS WHEN THE VERTICAL JUMPERS ARE REPOSITIONED?

ANSWER: _____
_____

6) RECORD THE WAVEFORM OF THE VERTICAL SYNC PULSE BELOW. INDICATE THE PULSE PERIOD.

7) CONNECT THE CH A PROBE TO PIN 1 OF U39 TO MEASURE SIGNAL "HDRV". CONNECT THE CH B PROBE TO PIN 13 OF U23 TO MEASURE SIGNAL "HSYNC".

8) SET THE SWEEPTIME/CM CONTROL ON THE OSCILLOSCOPE TO 5 MICROSECONDS.

9) THE LEFT EDGE OF THE OSCILLOSCOPE GRATICULE REPRESENTS THE LEADING EDGE OF SIGNAL "HDRV".

QUESTION 4. WHAT IS THE TIME DIFFERENCE BETWEEN THE LEADING EDGES OF SIGNALS "HDRV" AND "HSYNC"?

ANSWER: _____

10) RECORD THE WAVEFORM OF THE HORIZONTAL SYNC PULSE BELOW. INDICATE THE PULSE PERIOD.

THIS COMPLETES YOUR LAB ASSIGNMENT ON THE MODEL III VIDEO DISPLAY GENERATOR.

A.J. DEL ROSARIO
2/23/1982